SPECIFICATION AMENDMENTS

Insert the heading and paragraph at page 1, line 1 as follows:

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Application Serial No. 10/059,686 filed on January 29, 2002, which is a continuation of U.S. Application Serial No. 10/042,812 filed on January 9, 2002.

Replace the paragraph at page 5, lines 8-18 with the following paragraph:

In accordance with another aspect of the invention, a method of making a semiconductor package device includes attaching a semiconductor chip to a metallic structure using an insulative adhesive, wherein the chip includes a conductive pad, the metallic structure includes first and second opposing surfaces and a lead~~conductive trace~~, the adhesive is disposed between the first surface and the chip, the lead~~conductive trace~~ includes a recessed portion, a non-recessed portion and opposing outer edges between the first and second surfaces that extend across the recessed and non-recessed portions, and the recessed portion is recessed relative to the non-recessed portion at the second surface, forming an encapsulant that contacts the chip, the first surface, the outer edges and the recessed portion, wherein the encapsulant completely covers the chip, the outer edges and the recessed portion without completely covering the non-recessed portion, and forming a connection joint that electrically connects the lead~~conductive trace~~ and the pad.

Replace the paragraph at page 10, lines 5-14 with the following paragraph:

FIGS. 1A and **1B** are top and bottom perspective views, respectively, of semiconductor chip 110 which is an integrated circuit in which various transistors, circuits, interconnect lines and the like are formed (not shown). Chip 110 includes opposing major surfaces 112 and 114 and has a thickness of 200 microns between these surfaces. Surface 112 is an upper surface, and surface 114 is a lower surface. Surface 112 is the active surface and includes conductive pads

116 arranged in a single row and passivation layer 118. Pads 116 are substantially aligned with passivation layer 118 so that surface 112 is essentially flat. Alternatively, if desired, pads 116 can extend above or be recessed below passivation layer 118. Pads 116 provides bonding sites to electrically couple chip 110 with external circuitry. Thus, a particular pad 116 can be input/output pad or a power/ground pad. Pads 116 have a length and width of 70 microns.

Replace the paragraph at page 16, lines 10-13 with the following paragraph:

FIG. 5C is an enlarged plan view of encircled detail 5C in FIG. 5A that shows a representative pad 116 and routing line 148 in greater detail. Since pad 116 and routing line 148 are not ~~be~~ visible from surface 114 of chip 110, they are shown in phantom. Routing line 148 includes a distal end that overlaps pad 116.

Replace the paragraph at page 19, lines 27-31 with the following paragraph:

A suitable wet chemical etch can be provided by the same solution used to form slots 128 and recessed portions 130, 132 and 134. The optimal etch time for exposing the structure to the wet chemical etch without excessively exposing the portions of leads 138 embedded in peripheral portion 166 and adjacent to inner side surfaces 174 after the selected copper has been removed can be established through trial and error.

Replace the paragraph at page 23, line 23 to page 24, line 6 with the following paragraph:

At this stage, device 186 includes chip 110, conductive traces 150, adhesive 154, connection joints 180 and insulative housing 184. Conductive traces 150 each include a lead 138 that protrudes laterally from and extends through a side surface 162 of insulative housing 184, a terminal 146 that protrudes downwardly from and extends through bottom surface 164 of insulative housing 184, and a routing line 148 within insulative housing 184 that is integral with an associated terminal 146 and contacts an associated lead 138 and connection joint 180. Conductive traces 150 are electrically connected to pads 116 by connection joints 180 in one-to-one relation, and are electrically isolated from one another. Leads 138 are arranged in opposing rows that protrude laterally from and extend through opposing side surfaces 162 and are disposed between top surface 160 and bottom surface 164. Terminals 146 are arranged as an array that

protrudes downwardly from and extends through bottom surface 164 and is disposed inside inner side surfaces 174. Furthermore, leads 138 and terminals 146 are spaced and separated from one another outside insulative housing 184, and leads 138 and terminals 146 are electrically connected to one another and to pads 116 inside insulative housing 184 and outside chip 110.

Replace the paragraph at page 25, lines 16-24 with the following paragraph:

Advantageously, the present invention provides a semiconductor package device that has ~~have~~ a first electrode configuration for the test socket and a second electrode configuration for the next level assembly. The first electrode configuration is provided by the leads, and the second electrode configuration is provided by the terminals. As a result, the device is flexible enough to accommodate test sockets and printed circuit boards with different electrical contact requirements. In other words, the leads can be optimized for mating with the test socket, and the terminals can be optimized for mating with the next level assembly. In this manner, the device can be tested using a standard test socket, and then attached to a printed circuit board with an entirely different contact arrangement than the test socket.

Replace the paragraph at page 30, line 22 to page 31, line 9 with the following paragraph:

The connection joints can be formed from a wide variety of materials including copper, gold, nickel, palladium, tin, alloys thereof, and combinations thereof, can be formed by a wide variety of processes including electroplating, electroless plating, ball bonding, solder reflowing and conductive adhesive curing, and can have a wide variety of shapes and~~as~~ sizes. The shape and composition of the connection joints depends on the composition of the conductive traces as well as design and reliability considerations. Further details regarding an electroplated connection joint are disclosed in U.S. Application Serial No. 09/865,367 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Simultaneously Electroplated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding an electrolessly plated connection joint are disclosed in U.S. Application Serial No. 09/864,555 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding a ball bond connection joint are disclosed in

U.S. Application Serial No. 09/864,773 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Ball Bond Connection Joint" which is incorporated by reference. Further details regarding a solder or conductive adhesive connection joint are disclosed in U.S. Application Serial No. 09/927,216 filed August 10, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Hardened Connection Joint" which is incorporated by reference.

Replace the paragraph at page 32, lines 18-22 with the following paragraph:

For instance, if an optoelectronic chip is employed with a light sensitive cell and pads on the upper surface, the pads, adhesive, conductive traces and connection joints are disposed outside the light sensitive cell, and the insulative base is a transparent epoxy layer that is deposited on the light sensitive cell, then the light sensitive cell will receive~~be exposed to~~ light from the external environment that impinges upon and passes through the insulative base.